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Complete if Known

Application Number	10/716755
Filing Date	November 19, 2003
First Named Inventor	Tang, Stephen
Group Art Unit	2818 2827
Examiner Name	<del>Unknown</del> S. MAI

Sheet 1 of 1

Attorney Docket No: 80107.038US1

**US PATENT DOCUMENTS**

Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	Filing Date If Appropriate
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**FOREIGN PATENT DOCUMENTS**

Examiner Initials *	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	T <sup>2</sup>
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**OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS**

Examiner Initials *	Cite No *	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>1</sup>
JL		FAZAN, PIERRE, et al., "A Simple 1-Transistor Capacitor-Less Memory Cell for High Performance Embedded DRAMs", <u>IEEE 2002 Custom Integrated Circuits Conference</u> , (2002),99-102	
JH		OHSAWA, TAKASHI, et al., "A Memory Using One-Transistor Gain Cell on SOI(FBC) with Performance Suitable for Embedded DRAM's", <u>2003 Symposium on VLSI Circuits Digest of Technical Papers</u> , (2003),4 pages	
JM		OHSAWA, TAKASHI, et al., "Memory Design Using a One-Transistor Gain Cell on SOI", <u>IEEE Journal of Solid-State Circuits</u> , vol. 37, no. 11, (November 2002),1510-1522	
JM		OHSAWA, TAKASHI, et al., "Memory Design Using One-Transistor Gain Cell on SOI", <u>ISSCC 2002, Session 9, Dram and Ferroelectric Memories</u> , 9.1, (February 5, 2002),3 pages	
JM		OKHONIN, S., "A Capacitor-Less 1T-DRAM Cell", <u>IEEE Electron Device Letters</u> , vol. 23, no. 2, (February 2002),85-87	
JM		OKHONIN, S., et al., "A SOI Capacitor-less 1T-DRAM Concept", <u>2001 IEEE International SOI Conference</u> , (October 2001),153-154	

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SON MAI

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